REMARKS

Claims 1-5 are pending in the application.

The title of the invention has been objected to. A new title has been proposed herein.

Applicant's claimed invention relates to an interface device establishing an interface between a CPU and an external unit.

Claims 1-5 pending in the application are rejected under 35 U.S.C. § 102(e) as being anticipated by Evoy (U.S. Patent No. 6,062,480). Evoy teaches a hot docking system with a system comprising a card 28, a bus isolation circuit 18 having an interface unit to which the card 28 is detachably connected, and a CPU subsystem 26 to be connected to the bus isolation circuit 18 (see Fig. 1). It's asserted in the Office Action that the CPU, the external unit, and the interface device of applicant's claimed invention corresponds to the CPU subsystem 26, the card 28, and the bus isolation circuit 18, respectively of Evoy.

However, the bus isolation circuit 18 of Evoy does not teach nor suggest the timer portion of applicant's claimed invention that the interface device measures transmission time of the wait signal transmitted from the external unit to assert the mask signal when the wait signal kept being transmitted for more than a predetermined period of time.

Applicant's claimed invention includes the interface device which includes a timer portion, a mask portion and an interrupt portion. The timer asserts a mask signal when detecting that a wait signal continues to be outputted from the external unit for more than a predetermined period of time. The mask portion masks the wait signal outputted from the external unit when the mask signal is asserted. The interrupt portion issues an interrupt signal to the CPU when the mask signal is asserted. With this configuration, it is possible to prevent a system freeze even in

such a case that the failure or the like of the external unit keeps the wait signal being asserted and bus being occupied.

In contrast Evoy does not teach nor suggest such a timer portion as claimed by applicant. Because this feature is not found in Evoy it is respectfully requested the rejection be withdrawn.

Additionally of the bus isolation circuit 18 of Evoy (a buffer 18B included in the bus isolation circuit 18) to control a bus 22 is different from that of the mask portion of applicant's claimed invention.

In particular in Evoy the buffer 18B does not teach that the wait signal is masked to the control bus. Evoy makes such a description of the buffer 18B which is different from applicant's claimed invention. See column 3, lines 25 – 66; column 4, lines 50 – 64 of Evoy.

In contrast applicant claims the mask portion masks the wait signal to control the bus when the timer portion asserts the mask signal. Consequently, Evoy is completely different from and cannot achieve the above-mentioned advantage of the present claimed invention.

Applicant's claim 2 describes an information processing system comprising a CPU and an interface device for establishing an interface between the CPU and an external unit. When the interface device detects that a wait signal outputted from said external unit has been kept asserted for more than a predetermined period of time, said interface device masks the wait signal for outputting to said CPU and issues an interrupt signal to said CPU.

Thus claim 2 detects that a wait signal continues to be outputted from the external unit for more than a predetermined period of time. Likewise as in claim 1 this feature is not taught by Evoy. Dependent claims 3-5 include at least the distinguishing features of claim 2 and additional distinguishing features for example claim 3 includes a timer portion is activated when the wait signal outputted from the external unit is asserted, and then asserts a mask signal when the wait

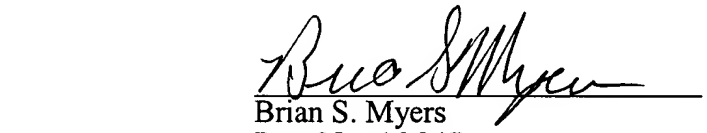
signal is kept asserted for more than a predetermined period of time, the mask portion masks the wait signal for outputting to said CPU when the mask signal is asserted.

For at least the foregoing reasons it is respectfully submitted that Evoy does not teach nor suggest the features of applicant's claimed invention. Therefore, the present invention is not anticipated by Evoy and the rejection should be withdrawn.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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